

**REMARKS**

In the non-final Office Action, the Examiner rejects claims 1-3 and 7 under 35 U.S.C. § 103(a) as unpatentable over HOOGENBOOM et al. (U.S. Patent Application Publication No. 2002/0054568) in view of ZHANG et al. ("Integrated Rate and Credit Feedback Control for ABR Service in ATM Networks," IEEE, 1997, Pages 1295-1303), and further in view of CARR et al. (U.S. Patent No. 6,643,293); rejects claims 4 and 9 under 35 U.S.C. § 103(a) as unpatentable over HOOGENBOOM et al. in view of ZHANG et al., and further in view of CARR et al. and KOZAKI et al. (U.S. Patent No. 6,389,026); rejects claims 5 and 6 under 35 U.S.C. § 103(a) as unpatentable over HOOGENBOOM et al. in view of ZHANG et al., and further in view of CARR et al. and ENDO et al. (U.S. Patent No. 6,275,494); and rejects claim 8 under 35 U.S.C. § 103(a) as unpatentable over HOOGENBOOM et al. in view of ZHANG et al., and further in view of CARR et al. and WATANABE (U.S. Patent No. 5,771,231). Applicants respectfully traverse these rejections. Claims 1-9 remain pending.

Claims 1-3 and 7 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over HOOGENBOOM et al. in view of ZHANG et al., and further in view of CARR et al. Applicants respectfully traverse this rejection.

Independent claim 1 recites a switch comprising one or more input side circuit interfaces; one or more output side circuit interfaces; and a core switch for outputting cells inputted thereto from said input side circuit interface or interfaces to said output side circuit interface or interfaces. Each of said output side circuit interfaces feeds back a cell number accumulated for each virtual channel to a corresponding one of said input side

circuit interfaces. Each of said input side circuit interfaces shapes the rate of cells based on the feedback from a corresponding one of said output side circuit interfaces so that a peak cell rate total value of virtual channels which belong to a virtual path may not exceed a peak cell rate of the virtual path. Each of said output side circuit interfaces controls, based on the cell number accumulated for each virtual channel, so that the peak cell rate of the virtual path to which the virtual channels belong may not exceed the peak cell rate total value of the virtual channels which belong to the virtual path.

HOOGENBOOM et al., ZHANG et al., and CARR et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, HOOGENBOOM et al., ZHANG et al., and CARR et al. do not disclose or suggest that each of the output side circuit interfaces feeds back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces. The Examiner relies on para. 0026; para. 0028, lines 1-10; para. 0034, lines 12-20; and signal 525 in Fig. 5 of HOOGENBOOM et al. for allegedly disclosing this feature of claim 1 (Office Action, pg. 3). Applicants respectfully disagree with the Examiner's interpretation of HOOGENBOOM et al.

At para. 0026, HOOGENBOOM et al. discloses:

In order to implement an appropriate priority-based congestion control strategy and an appropriate connection-based congestion control strategy in the ATM switch according to FIG. 3, output control 350 must know the present backlog of data units the P stores in data buffer 340. For this purpose, P physical memories are provided within output control 350. Each time a data unit is buffered in one of the P stores within data buffer 340, output control 350 increments a backlog value in a memory corresponding to the store so that the current backlog of data units stored in each store is determinable by output control 350 by reference to the incremented value. If desired, output control 350 may maintain a global

backlog value reflecting the aggregate backlog of data units awaiting access to output port 330.

This section of HOOGENBOOM et al. discloses that each time a data unit is buffered in one of the P stores within data buffer 340, output control 350 increments a backlog value in a memory corresponding to the store so that the current backlog of data units stored in each store is determinable by output control 350 by reference to the incremented value. This section of HOOGENBOOM et al. in no way relates to each of one or more output side circuit interfaces feeding back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces, as required by claim 1. In fact, this section of HOOGENBOOM et al. does not disclose or suggest that output control 350 feeds back any information to input side circuit interfaces.

At para. 0028, lines 1-10, HOOGENBOOM et al. discloses:

The basic connection-based congestion control strategy implemented by output logic unit 320 in may be described by reference to FIG. 7A. Whenever a data unit is added to data buffer 340, output control 350 increments the backlog value of the corresponding store. Output control 350 monitors the P backlog values (700) and compares any one, any desired combination, or all of the backlog values with selected maximum values to determine if a maximum value has been exceeded (710). If a maximum value has been exceeded and a rate limitation is not presently being.

This section of HOOGENBOOM et al. discloses that whenever a data unit is added to data buffer 340, output control 350 increments a backlog value of the corresponding store and may compare the backlog value to a maximum value. This section of HOOGENBOOM et al. in no way relates to each of one or more output side circuit interfaces feeding back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces, as required by claim 1. In fact, this

section of HOOGENBOOM et al. does not disclose or suggest that output control 350 feeds back any information to input side circuit interfaces.

Applicants note that at para. 0028, lines 10-13, HOOGENBOOM et al. discloses that output control 350 transmits an activation congestion control signal to rate filter 360 when a backlog value exceeds a maximum value and a rate limitation is not presently being enforced by rate filter 360. HOOGENBOOM et al. does not disclose or suggest, however, that the activation congestion control signal includes a cell number accumulated for each virtual channel, as would be required by claim 1. Moreover, one skilled in the art would readily appreciate that rate filter 360 cannot reasonably be construed to correspond to an input side circuit interface since rate filter 360 is located in output logic unit 320. Applicants submit that neither this paragraph of HOOGENBOOM et al. nor any other section of HOOGENBOOM et al. discloses or suggests each of one or more output side circuit interfaces feeding back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces, as required by claim 1.

At para. 0034, lines 12-20, HOOGENBOOM et al. discloses:

If a maximum value has been exceeded and a rate limitation is not presently being enforced by rate filter 570, output control 580 transmits an "activate congestion control" signal to input control 560 on line 525 instructing input control 460 to have rate filter 570 enforce a rate limitation. If a maximum value has not been exceeded and a rate limitation is presently being enforced by rate filter 570, output control 580 transmits a "deactivate congestion control" signal to input control 560 on line 525.

Similar to the above section of HOOGENBOOM et al., this section of HOOGENBOOM et al. discloses that output control 580 transmits an activation congestion control signal to input control 560 on line 525 (Fig. 5) when a backlog value exceeds a maximum value.

HOOGENBOOM et al. does not disclose or suggest that the activation congestion control signal includes a cell number accumulated for each virtual channel, as would be required by claim 1.

The Examiner admits that HOOGENBOOM et al. does not disclose "a buffering arrangement where the output sends a total cell count of each virtual connection to the corresponding input side for congestion monitoring." (Office Action, pg. 5). Applicants submit that claim 1 does not recite a buffering arrangement where the output sends a total cell count of each virtual connection to the corresponding input side for congestion monitoring. Instead, claim 1 specifically recites that each of the output side circuit interfaces feeds back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces. Applicants respectfully submit that the Examiner has mischaracterized the above feature of claim 1. Moreover, it is unclear how the Examiner can rely on HOOGENBOOM et al., on the one hand, for allegedly disclosing the above feature of claim 1, and then admit, on the other hand, that HOOGENBOOM et al. does not disclose the same feature of claim 1.

Nevertheless, the Examiner alleges that "Zhang discloses a buffering arrangement where the *output* sends a total cell count of each virtual connection to the corresponding input side for congestion monitoring," and points to Fig. 1, Tables 1 and 3, pg. 1296, col. 2, lines 1-10, and pg. 1298, col. 2, lines 1-5, of ZHANG et al. for support (Office Action, pg. 6). Applicants submit that the Examiner's allegation does not address the above feature of claim 1. As set forth above, claim 1 does not recite a buffering arrangement where the output sends a total cell count of each virtual connection to a corresponding

input side for congestion monitoring. Instead, claim 1 specifically recites that each of the output side circuit interfaces feeds back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces. The Examiner's allegation does not address this specifically recited feature.

Nevertheless, in Fig. 1, ZHANG et al. depicts the transmission of an explicit forward congestion indication (EFCI) bit from a source end system through a group of switches to a destination end system and the transmission of resource management (RM) cells from the destination end system through the group of switches to the source end system. Fig. 1 of ZHANG et al. in no way discloses or suggests that one of the switches in the group of switches includes one or more input side circuits and one or more output side circuits, where each of the one or more output side circuit interfaces feeds back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces, as required by claim 1. In fact, neither Fig. 1 nor the description thereof discloses or suggests the contents of any of the switches in the group of switches depicted in Fig. 1.

Tables 1 and 3 in ZHANG et al. describe operations performed by a source node and a destination node, respectively. Table 1 discloses two events that are performed by the source node: sending data cells and receiving RM cells (pg. 1297, col. 2). Table 3 discloses two events that are performed by the destination node: receiving data cells and receiving RM cells (pg. 1298, cols. 1-2). ZHANG et al. discloses that the RM cells include a direction (DIR) bit, a backward notification (BN) bit, a congestion indication (CI) bit, a two-byte explicit cell rate (ER) field, a two-byte current cell rate (CCR) field, a

two-byte minimum cell rate (MCR) field, and a two-byte credit update (CU) value field. ZHANG et al. does not disclose or suggest that the RM cells include a cell number accumulated for each virtual channel or that each of the one or more output side circuit interfaces of a switch feeds back a cell number accumulated for each virtual channel in an RM cell (or in any other manner) to a corresponding one of the input side circuit interfaces of the switch, as would be required by the Examiner's interpretation of claim 1.

At pg. 1296, col. 2, lines 1-10, ZHANG et al. discloses that using RM cells and an EFCI bit setting, the information feedback control loop spans the entire network in an end-to-end fashion. This section of ZHANG et al. does not disclose or suggest a switch that includes one or more input side circuits and one or more output side circuits, where each of the one or more output side circuit interfaces feeds back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces, as required by claim 1.

At pg. 1298, col. 2, lines 1-5, ZHANG et al. discloses that when a data cell is received, its EFCI bit is saved and the local count is updated. This section of ZHANG et al. does not disclose or suggest a switch that includes one or more input side circuits and one or more output side circuits, where each of the one or more output side circuit interfaces feeds back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces, as required by claim 1.

The disclosure of CARR et al. does not remedy the above deficiencies in the disclosures of HOOGENBOOM et al. and ZHANG et al.

Since HOOGENBOOM et al., ZHANG et al., and CARR et al. do not disclose or

suggest each of the one or more output side circuit interfaces feeding back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces, as required by claim 1, HOOGENBOOM et al., ZHANG et al., and CARR et al. cannot disclose or suggest each of the input side circuit interfaces shaping the rate of cells based on the feedback from a corresponding one of the output side circuit interfaces so that a peak cell rate of the virtual path to which the virtual channels belong may not exceed the peak cell rate total of the virtual channels which belong to the virtual path, as also required by claim 1.

For at least the foregoing reasons, Applicants submit that claim 1 is patentable over HOOGENBOOM et al., ZHANG et al., and CARR et al., whether taken alone or in any reasonable combination.

Claims 2 and 3 depend from claim 1. Therefore, these claims are patentable over HOOGENBOOM et al., ZHANG et al., and CARR et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1. Moreover, these claims recite additional features not disclosed or suggested by HOOGENBOOM et al., ZHANG et al., and CARR et al.

For example, claim 2 recites that each of the input side circuit interfaces includes a physical layer processing section which terminates a cell, and an input virtual channel cell rate control section for receiving the cell terminated by said physical layer processing section and controlling the rate of cell for each virtual channel based on the feedback. HOOGENBOOM et al., ZHANG et al., and CARR et al. do not disclose or suggest this combination of features.



For example, since HOOGENBOOM et al., ZHANG et al., and CARR et al. do not disclose or suggest feeding back a cell number accumulated for each virtual channel to a corresponding one of the input side circuit interfaces, HOOGENBOOM et al., ZHANG et al., and CARR et al. cannot disclose or suggest an input virtual channel cell rate control section for receiving the cell terminated by the physical layer processing section and controlling the rate of cell for each virtual channel based on the feedback, as required by claim 2. The Examiner relies on elements 520 and 525 in Fig. 5 and para. 0031 of HOOGENBOOM et al. for allegedly disclosing the above feature of claim 2 (Office Action, pp. 3 and 4). Applicants respectfully disagree with the Examiner's interpretation of HOOGENBOOM et al.

Elements 520 and 525 in HOOGENBOOM et al.'s Fig. 5 correspond to an input logic unit and a line that connects an input control 560 to an output control 580, respectively. HOOGENBOOM et al. discloses that when a backlog value exceeds a maximum value and a rate limitation is not presently being enforced by rate filter 570, output control 580 transmits an activation congestion control signal to input control 560 in input logic unit 520 on line 525 instructing input control 560 to have rate filter 570 enforce a rate limitation (para. 0034). HOOGENBOOM et al. in no way discloses or suggests that the activation congestion control signal, which the Examiner alleges corresponds to the recited feedback, includes a cell number accumulated for each virtual channel, as would be required by claim 2.

At para. 0031, HOOGENBOOM et al. discloses:

Turning now to FIG. 5, the flows between any input port and output port in a DIBOC-based ATM switch in accordance with the more preferred

embodiment are generalized by reference to the flows between input port 510 and output port 540. Input logic unit 520 is fed by input port 510, which may at different times in an operational cycle support different virtual connections delivering data units at different rates. Input logic unit 520 is arranged to feed output logic unit 540. Input logic unit 520 includes a data buffer 550 which feeds output port 540, and an input control 560 and rate filter 570. Output logic unit 530 includes an output control 580 which monitors the bandwidth at output port 540. Data buffer 550 has operatively distinct stores for buffering data units according to different characteristics, such as destination output port and priority. For a switch having O output ports and supporting P levels of priority, data buffer 550 preferably has O×P stores for separately buffering data units for any destination output port and priority combination, and P stores for separately buffering data units for a particular destination output port and any priority. Input control 560 segregates unfiltered data units received at input port 510 for storage within one of its O×P stores, and more particularly within one of the P stores associated with the destination output port. Upon prompting from the output logic unit associated with the destination output port, input control 560 eventually releases the buffered data units from the store to the destination output port. In a DIBOC-based ATM switch with I input ports, there will, naturally, be in the aggregate I×P stores associated with a particular destination output port and any priority.

This section of HOOGENBOOM et al. discloses that input control 560 releases buffered data units to the destination output port in response to prompting by the output logic unit associated with the destination output port. This section of HOOGENBOOM et al. does not disclose or suggest an input virtual channel cell rate control section for receiving the cell terminated by the physical layer processing section and controlling the rate of cell for each virtual channel based on a cell number accumulated for each virtual channel received from an output side circuit interface, as required by claim 2.

For at least these additional reasons, Applicants submit that claim 2 is patentable over HOOGENBOOM et al., ZHANG et al., and CARR et al., whether taken alone or in any reasonable combination.

Independent claim 7 recites features similar to, yet possibly of different scope than, features set forth above with respect to claim 1. For example, claim 7 recites an input processing section configured to output cells for each virtual channel at a rate equal to or higher than a minimum cell rate based on a control signal, where the control signal indicates a determined number of cells stored for each VC. HOOGENBOOM et al., ZHANG et al., and CARR et al. do not disclose or suggest this feature. Applicants submit that claim 7 is patentable over HOOGENBOOM et al., ZHANG et al., and CARR et al., whether taken alone or in any reasonable combination, for at least reasons similar to reasons given above with respect to claim 1.

Claims 4 and 9 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over HOOGENBOOM et al., ZHANG et al., CARR et al., and KOZAKI et al. Applicants respectfully traverse this rejection.

Claim 4 depends from claim 1. The disclosure of KOZAKI et al. does not remedy the deficiencies in the disclosures of HOOGENBOOM et al., ZHANG et al., CARR et al. set forth above with respect to claim 1. Therefore, claim 4 is patentable over HOOGENBOOM et al., ZHANG et al., CARR et al., and KOZAKI et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1.

Claim 9 depends from claim 7. The disclosure of KOZAKI et al. does not remedy the deficiencies in the disclosures of HOOGENBOOM et al., ZHANG et al., CARR et al. set forth above with respect to claim 7. Therefore, claim 9 is patentable over HOOGENBOOM et al., ZHANG et al., CARR et al., and KOZAKI et al., whether taken

alone or in any reasonable combination, for at least the reasons given above with respect to claim 7.

Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over HOOGENBOOM et al., ZHANG et al., CARR et al., and ENDO et al. Applicants respectfully traverse this rejection.

Claims 5 and 6 depend from claim 2. The disclosure of ENDO et al. does not remedy the deficiencies in the disclosures of HOOGENBOOM et al., ZHANG et al., and CARR et al. set forth above with respect to claim 2. Therefore, claims 5 and 6 are patentable over HOOGENBOOM et al., ZHANG et al., CARR et al., and ENDO et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 2.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over HOOGENBOOM et al., ZHANG et al., CARR et al., and WATANABE. Applicants respectfully traverse this rejection.

Claim 8 depends from claim 7. The disclosure of WATANABE does not remedy the deficiencies in the disclosures of HOOGENBOOM et al., ZHANG et al., and CARR et al. set forth above with respect to claim 7. Therefore, claim 8 is patentable over HOOGENBOOM et al., ZHANG et al., CARR et al., and WATANABE, whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 7.

In view of the foregoing remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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